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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/740,469	12/22/2003	Kouichi Takagi	118153	3615

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/740,469	TAKAGI ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1 pg*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 are rejected under 35 U.S.C. 103(b) as being anticipated by Kasai (US 6116916) in view of Okada et al. (US 6534726, hereinafter "Okada").

Regarding claim 1, as shown in figure 1, Kasai disclose a control circuit board (considering PCB 23 including insulating plate 27 as a control circuit board, see col.4:1-8) comprising:

(a) A plurality of bus bars 24 (col.4:4) that are bonded to a surface of the control circuit board in a state that the bus bars 24 are arranged approximately in the same plane; and

(b) a connection portion 27a/23d/24b (terminal holes and male terminals, col.4:42-58; the connecting portions 27a/23d are formed near an edge of the circuit board) to be connected to an external circuit.

But, Kasai fails to disclose the connecting portion is configured such that an end portion of the control circuit board is formed with a cut which is opened sideways and is coated with a general semi-circular conductor layer in such a manner that an inner side

surface of the cut is covered with the conductor layer, an inner circumferential surface of the conductor layer is connected to a circuit that is incorporated in the control circuit board.

Okada, as shown in figures 3-4 and 8, discloses a circuit board 11 (a module substrate) having electronic components and circuit patterns formed thereon (figures 1 and 8, col.7:1-12 and col.2:18-28). The circuit board 11 has a connecting portion 13 (end-face through-hole) for connecting to a circuit element formed on another circuit board (a mother board) by solder 17/18 (solder/fillet, col.7:34-48). The connecting portion 13 is configured such that an end portion of the board 11 is formed with a cut 14 (an end-face opening groove, col.7:13-18) which is opened sideways and is coated with a general semi-circular conductor layer 15 (end-face electrode) in such a manner that an inner side surface of the cut 14 is covered with the conductor layer 15, an inner circumferential surface of the conductor layer (clearly shown in figures 3-4) is connected to a circuit 16 (wiring, the circuit formed on the board 11, col.7:27-33) that is incorporated in the circuit board 11.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the teachings about the connecting portion 13 from Okade on the board of Kasai that the connecting portion 27a/23d of Kasai is configured such that an end portion of the control circuit board is formed with a cut 14 (taught by Okada) which is opened sideways (at the edge of the board) and is coated with a general semi-circular conductor layer 15 (taught by Okada) in such a manner that an inner side surface of the cut 14 is covered with the conductor layer 15 (taught by Okada), an inner

circumferential surface of the conductor layer is connected to a circuit (the circuit of the PCB 23) that is incorporated in the control circuit board in order to easily visually inspect the connection between the terminals 24d and the control circuit board.

Examiner remarks: It is noted that the teachings from Okada is centering about an edge connection portion of a substrate that are not limited to a connection between a substrate to a pad formed on another board. Therefore, it is understood that the teachings is not limited to a pad itself but also to any conductive layer.

Regarding claim 2, Kasai (as shown in figure 1) in view of Okada (as shown in figures 3-4 and 8) discloses every limitation as shown in claim 1 above including a circuit structural body comprising:

(a) A plurality of bus bars 24 that are part of a power circuit (part of the power circuit of a automotive vehicle junction box, col.1:4-9),

(b) the power circuit are bonded to a surface of a control circuit board 23 in a state that the bus bars 24 are arranged approximately in the same plane,

(c) the control circuit board 23 including a connecting portion 13 (taught by Okada) to be connected to an external circuit, the connecting portion is configured such that an end portion of the control circuit board is formed with a cut 14 (taught by Okada) which is opened sideways and is coated with a generally semi-circular conductor layer 15 (taught by Okada) in such a manner that an inner side surface of the cut 14 is covered with the conductor layer 15, the conductor layer 15 is connected to a circuit (control circuit of the junction box) that is incorporated in the control circuit board 23,

(d) wherein a particular one of the bus bars 24 (section of terminal 24b) is electrically connected to the circuit incorporated in the control circuit board 23 by soldering 17 (formed into fillet 18, col.7:34-48, the teaching from Okada) in which solder 17 is supplied so as to bridge an inner circumferential surface of the conductor layer 15 of the control circuit board and a surface of the particular one of the bus bar 24 in a state that a coating portion of the conductor layer is laid on the particular bus bar.

Regarding claim 3, Kasai in view of Okada discloses every limitation as shown in claim 2 above and inherently including a switching element (every electrical junction box has switch element), which is provided in the power circuit including the bus bars 24, the control circuit board 23 incorporates a control circuit for controlling driving of the switching element (the purpose of the PCB 23), and the switching element is mounted so as to bridge the bus bar 24 and the control circuit board 23 (because the switch element must be electrically connected the bus bar and also the control circuit, therefore at least one gate of the switch is connected to the bus bars and at least one gate is connected to the control circuit of the board 23).

Examiner remarks: It is noted that the Examiner considers the connections of the switch element (key element in every junction box, a high power MOSFET for example) contain at least one gate connected to a bus bar (a high power circuit traces) and at least one gate connected to a control circuit (controlling the switch element). And, this is the basic connection in every electrical junction box. The Examiner broadly considers the connection as a "bridge", because the claim fails to recite any structure limitation with the regard to the bridge that would keep the claim from reading on the

interpretation of the reference that a connection between the switch, the bus bar, and the control circuit can be considered as a "bridge".

Regarding claim 4, Kasai (as shown in figure 1) in view of Okada (as shown in figures 3-4 and 8) discloses every limitation as shown in claim 2 above including a plurality of bus bars 24 (section of terminal 24b) project sideways from the control circuit board 23 to serve as terminals to be connected to the external circuit, and at least part of the bus bars to serve as the terminals that are electrically connected to the conductor layers 15 by soldering 17.

Regarding claim 5, Kasai (as shown in figure 1) in view of Okada (as shown in figures 3-4 and 8) discloses every limitation as shown in claims 2 and 4 above including the bus bars 24 to serve as the terminals (24b) that are bent in the same direction (a section of the terminal is bent upward) that is generally perpendicular to the control circuit board 23.

Regarding claim 6, Kasai (as shown in figure 1) in view of Okada (as shown in figures 3-4 and 8) discloses every limitation as shown in claims 2 and 4 above and inherently including the terminals 24b that include signal input terminals to which instruction signals are input externally, and the bus bars to serve as the signal input terminals are electrically connected to the conductor layers 15 (the teaching from Okada).

Response to Arguments

4. Applicant's arguments (filed on 6/5/06) with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment of 6/5/06 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). DR 12/8/06

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
12/4/06

Dean A. Reichard 12/8/06
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